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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,603	03/15/2004	Tomoo Yamasaki	CU-3637 RJS	1812

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EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,603	YAMASAKI ET AL.	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hale et al (U.S. Patent #6407929), in view of Sweterlitsch (U.S. Patent #6737742).

With respect to **claims 1-6**, Hale teaches a substrate body (Fig. 3, 302) having a wiring layer (Fig. 3, 306), and a reinforcing member provided in said substrate body and reinforcing said substrate body (Fig. 3, 310);

that the reinforcing member is a circuit board having a capacitor part that electrically connects the semiconductor element and the wiring layer (Fig. 10, 1004), as set forth in claim 2;

that the reinforcing member is an interposer having a via (Fig. 3, 312) that directly electrically connects the semiconductor element (Fig. 3, 314) and the wiring layer (Fig. 3, 306), as set forth in claim 4;

Hale does not teach a base formed by a material that is different from a material of said substrate body, supporting said substrate body, and having an opening forming portion where a semiconductor element is mounted, as set forth

in claim 1; that the reinforcing member is arranged on the base via an abutting member made of a metal, as set forth in claims 3, 5, and 6.

Sweterlitsch teaches a base formed by a material that is different from a material of said substrate body, supporting said substrate body, and having an opening forming portion where a semiconductor element is mounted (Fig. 1, 240), as set forth in claim 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a base supporting the substrate body of Hale wherein the reinforcing member is larger than the opening forming portion as taught by Sweterlitsch, and to arrange the reinforcing member on the base via an abutting member made of metal (Fig. 3, top layer of 302 in Hale) in order to protect the semiconductor element mounted therein.

With respect to **claims 7-12**, Hale teaches the manufacturing of a reinforcing member (Fig. 3, 310), forming a substrate body so that the reinforcing member is provided in said substrate (Fig. 3, 302), said substrate body including a wiring layer (Fig. 3, 306)

the step of manufacturing the reinforcing member includes a step of forming a capacitor on a core member (Fig. 3, 308), as set forth in claim 8;

the step of manufacturing the reinforcing member includes a step of forming a via penetrating the core member (Fig. 3, via penetrating layer 304), as set forth in claim 9.

Hale does not teach arranging the reinforcing member on a base at a portion corresponding to an opening forming portion of the base, or forming the opening forming portion smaller than the reinforcing member, thereby exposing a part of the reinforcing member at the opening forming portion, as set forth in claim 1; or that the reinforcing member is arranged on the base via an abutting member made of metal, as set forth in claims 10, 11, and 12.

Sweterlitsch teaches a base arranged on a substrate with an opening forming portion that is smaller than the substrate and exposes the substrate, and is made of a material that is different from a material of the base (Fig. 1, 240), as set forth in claim 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a base on the reinforcing member of Hale such that the opening forming portion is smaller than the reinforcing member and exposes the reinforcing member as taught by Sweterlitsch, and to arranged the reinforcing member on the base via an abutting member made of metal (Fig. 3, top layer of 302 in Hale), in order to protect the semiconductor element therein.

With respect to **claims 13-18**, Hale teaches a substrate body having a wiring layer (Fig. 3, 306), and a reinforcing member provided in said substrate body and reinforcing said substrate body (Fig. 3, 310), and a semiconductor element mounted on the substrate (Fig. 3, 314);

that the reinforcing member is a circuit board having a capacitor part that electrically connects the semiconductor element and the wiring layer (Fig. 10, 1004), as set forth in claim 14;

that the reinforcing member is an interposer having a via (Fig. 3, 312) that directly electrically connects the semiconductor element (Fig. 3, 314) and the wiring layer (Fig. 3, 306), as set forth in claim 16;

Hale does not teach a base formed by a material that is different from a material of said substrate body, supporting said substrate body, and having an opening forming portion where a semiconductor element is mounted, as set forth in claim 1; that the reinforcing member is arranged on the base via an abutting member made of a metal, as set forth in claims 15, 17, and 18.

Sweterlitsch teaches a base formed by a material that is different from a material of said substrate body, supporting said substrate body, and having an opening forming portion where a semiconductor element is mounted (Fig. 1, 240), as set forth in claim 13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a base supporting the substrate body of Hale wherein the reinforcing member is larger than the opening forming portion as taught by Sweterlitsch, and to arrange the reinforcing member on the base via an abutting member made of metal (Fig. 3, top layer of 302 in Hale) in order to protect the semiconductor element mounted therein.

With respect to **claim 19**, Hale teaches a substrate body having a wiring layer (Fig. 10, 1008), and a reinforcing member embedded in said substrate body and reinforcing said substrate body (Fig. 10, middle layer), and a semiconductor element mounted on the substrate (Fig. 10, 1004). Hale does not teach a base formed by a material that is different from a material of said substrate body, supporting said substrate body, and having an opening forming portion where a semiconductor element is mounted. Sweterlitsch teaches a base formed of a material that is different from a material of said substrate body, supporting said substrate body, and having an opening forming portion where a semiconductor element is mounted (Fig. 1, 240). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a base supporting said substrate body of Hale as taught by Sweterlitsch in order in protect the semiconductor element therein.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800